



CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

AC TESTING OF LEAKAGE CURRENT

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The paragraph beginning on page 5, line 6.

Pin to Vcc or Pin to Vss test

In general, at the beginning of the test, a pin is tri-stated or floated. The pin is subsequently driven to a known state with a Boundary Scan pattern (Vss, Vcc, low, or high) for a first predetermined time. After the pin reaches the known state, it is allowed to float or to be unconnected. If the pin has the defect being tested for, it leaks and eventually changes from one state to the other state. At a second predetermined time, the pin is sampled with Boundary Scan. In other words, the voltage value of the pin is measured by internal circuitry of the IC to determine its state at the second predetermined time. Based on the state (measured voltage) of the pin, a pass/fail result is determined. In the following detailed description, for simplicity, only leakage testing of pin 122-0 is described; other pins (122 1-N) are tested in the same manner. In one embodiment, only input/output pins of IC 120 are tested with Boundary Scan.

The paragraph beginning on page 8, line 27.

When pins 122-0 and 122-1 reach opposite states of Vcc and Vss, they are allowed to float. Pins 122-0 and 122-1 start to leak toward $V_{cc}/2$. At a second predetermined time, tester 110 samples the state each of the pins using Boundary Scan. In one embodiment, sampling the state of each of the pins 122-0 and 122-1 includes measuring a voltage value of each of the pins 122-0 and 122-1. Based on the states or the measured voltage values of pins 122-0 and 122-1, the quality or pass fail result of pins 122-0 122-1 are determined. Pin to Pin leakage test is further understood with a description of Figure 5.